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TITLE: Method for forming interlayer dielectric layer
of semiconductor device

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PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE
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KR 2001055915 A	July 4, 2001	N/A
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APPLICATION-DATA:

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INT-CL (IPC): H01L021/312

ABSTRACTED-PUB-NO: KR2001055915A

BASIC-ABSTRACT:

NOVELTY - A method for forming an interlayer dielectric layer of a semiconductor device is provided to prevent the formation of voids as well as the etch of an underlying layer.

DETAILED DESCRIPTION - The method includes forming an etch stopper(300) on a wafer(100) where a pattern(200) is preformed, then forming the first insulating layer(500) on the etch stopper(300) by flowing at least two source gases having different time for stabilization, then forming the second insulating layer(400) on the first insulating layer(500) by the source gases, and then flowing oxygen and hydrogen over a resultant structure in a temperature of 800-900deg. C and

for 10-60 seconds. The source gases may preferably use boron and phosphorus.

In addition, the first insulating layer(500) is a boro silicate glass(BSG)

layer with a thickness of 10-150 Angstrom , while the second insulating

layer(400) is a boro phospho silicate glass(BPSG) layer. The etch stopper(300)

is a silicon nitride layer.

CHOSEN-DRAWING: Dwg.1/10

TITLE-TERMS: METHOD FORMING INTERLAYER DIELECTRIC LAYER SEMICONDUCTOR DEVICE

DERWENT-CLASS: L03 U11

CPI-CODES: L04-C12B; L04-C12D;

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